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EXAMINER
KILDAY, LISA A

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/884,736	Applicant(s) CATABAY ET AL.
	Examiner Lisa A Kilday	Art Unit 2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/26/01 (IDS)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *17-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2-6*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Election/Restrictions

This application contains claims directed to the following patentably distinct species of the claimed invention:

-Species I: process for forming an integrated structure (figs. 1-6)

-Species II: process for forming a double damascene structure (figs. 7-11).

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over

the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

During a telephone conversation with John Taylor on 7/24/02 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-16. Affirmation of this election must be made by applicant in replying to this Office action. Claims 17-21 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

Update U.S. Patent Nos. under the heading: Cross References to Related Applications and on pg. 8, last paragraph.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (6,028,015). In re claim 1, Wang et al. discloses a process for forming an

integrated circuit structure having at least one layer of low k material therein and a layer, formed from a low k dielectric layer, suitable for use as an etch stop and/or an etch mask which comprises: forming a first layer of low k dielectric material (10) over a previously formed integrated circuit structure (2); and treating the upper surface of said first layer of low k dielectric material with a plasma to form a first layer of densified dielectric material (14, 18)over the remainder of the underlying first layer of low k dielectric material (fig. 4, col. 2 lines 43-56, col. 3 lines 43-49); whereby said first layer of densified dielectric material (18) is capable of serving as a etch stop and/or an etch mask (fig. 3 ref. 18) for etching of said underlying first layer of low k dielectric material.

In re claim 2, Wang et al. discloses the process of claim 1 including the further step of patterning said first layer of densified dielectric material to form a first etch mask layer of densified dielectric material (fig. 3 ref. 18) having a pattern of openings (12) therein suitable for use in etching a corresponding pattern of openings in said underlying first layer of low k dielectric material (col. 6 lines 4-10).

In re claim 3, Wang et al. discloses the process of claim 2 including the further step of etching said pattern of openings in said first layer of low k dielectric material through said pattern of openings in said first etch mask layer of densified dielectric material thereon (col. 6 lines 9-15).

In re claim 5, Wang et al. discloses the process of claim 3 wherein said pattern of openings etched in said first layer of low k dielectric material comprises a pattern of vias (12) extending through said first layer of low k dielectric material down to said previously formed integrated circuit structure (col. 6 lines 8-10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 6-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. in view of Yau et al. (6,054,379). In re claim 4, Wang et al. discloses the process of claim 3 however does not teach wherein said pattern of openings etched in said first layer of low k dielectric material through said first etch mask layer comprises a pattern of trenches extending through said first layer of low k dielectric material down to said previously formed integrated circuit structure. However, Yau et al. teaches wherein said pattern of openings (516) etched in said first layer of low k dielectric material (510) through said first etch mask layer (514) comprises a pattern of trenches (520) extending through said first layer of low k dielectric material (fig. 8f) down to said previously formed integrated circuit structure (512). Therefore it would be obvious to one skilled in the art at the time of invention to modify the process of Wang et al. and form trenches etched in first layer of low k dielectric material and through said first etch mask layer as taught by Yau et al. because said first etch mask layer is used to form trenches.

In re claim 6, Wang et al. teaches forming a densified dielectric material. However Wang et al. does not teach forming a second layer of low k dielectric material over said first layer of densified dielectric material. However Yau et al. teaches including the further step of forming a second layer of low k dielectric material (518) over said first

layer of densified dielectric material (514), (col. 12 lines 25-30). Therefore, it would be obvious to one skilled in the art at the time of the invention to modify the process of Wang et al. and deposit a second layer of low k dielectric material over said first layer of densified dielectric material as taught by Yau et al. because a second dielectric layer is deposited to help pattern trenches with the first layer of densified dielectric material.

In re claim 7 adds the limitation that the process of claim 6 includes that a capping layer is formed over the second layer of low k dielectric. Wang et al. teaches forming a second layer of k dielectric. However Wang et al. does not teach forming a protective capping layer over said second layer of low k dielectric. However Yau et al. teaches the process of claim 6 including the further steps of: forming a protective capping layer (718) of silicon oxide (col. 2 lines 45-48) over said second layer of low k dielectric material (714); forming over said protective capping layer of silicon oxide (col. 2 lines 45-48) a further etch mask (726) having a pattern of openings therein; and etching a pattern of openings in said capping layer through said further etch mask; removing said further etch mask (fig. 10F); and etching said second layer of low k dielectric material (714) through said pattern of openings in said protective capping layer, with said first layer of densified material acting as an etch stop (fig. 10F). Therefore it would be obvious to one skilled in the art at the time of invention modify the process of Wang et al. and to use the densified dielectric layers as etch stop layers, adhesive layers, liners, or cap layers due to their excellent barrier properties as taught by Yau et al.

Claim 8 adds the limitation that the process of claim 6 including the further step of treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material. However Wang et al. does not teach forming a second layer of densified dielectric material over said second low k dielectric material. However, Yau et al. teaches forming a second layer of densified dielectric material (524) over said second low k dielectric material (518). Therefore, it would be obvious to one skilled in the art at the time of the invention to modify the process of Wang et al. and to form a second layer of densified dielectric over a second low k dielectric material as taught by Yau et al. because the second layer of densified low k dielectric layer would inhibit absorption of moisture.

Claim 9 adds the limitation of the process of claim 8 including the further steps of: a) patterning said second layer of densified dielectric material to form a second etch mask layer of densified dielectric material over said second layer of low k dielectric material, said second etch mask layer having a pattern of openings therein suitable for use in etching a corresponding pattern of openings in the underlying second layer of low k dielectric material (518); and b) etching a pattern of openings in said second layer of low k dielectric material through said pattern of openings in said second etch mask layer, with said first layer of densified dielectric material serving as an etch stop. However Wang et al. does not teach forming a second layer of densified dielectric material. However Yau et al. teaches the further steps of: a) patterning said second layer of densified dielectric material to form a second etch mask layer of densified

dielectric material (524) over said second layer of low k dielectric material (fig. 8G), said second etch mask layer having a pattern of openings therein suitable for use in etching a corresponding pattern of openings in the underlying second layer of low k dielectric material (col. 12 lines 29-45); and b) etching a pattern of openings in said second layer of low k dielectric material (518) through said pattern of openings in said second etch mask layer, with said first layer of densified dielectric material serving as an etch stop (fig. 8H, col. 12 lines 45-48). Therefore it would be obvious to one skilled in the art modify the process of Wang et al. and to etch openings in the second layer of low k dielectric material using the second layer of densified dielectric material as an etch mask as taught by Yau et al. because the second layer of densified dielectric material would prevent metal migration into the surrounding dielectric material.

Claim 10 adds the limitation of the process of claim 9, including the further steps of: a) forming a pattern of openings in said first etch mask layer through said pattern of openings formed in said second layer of low k dielectric material; and b) etching a pattern of openings in said first layer of low k dielectric material through said pattern of openings in said first etch mask layer. Wang et al. teaches etching a pattern of openings in said first layer of low k dielectric material. However Wang et al. does not teach forming a second layer of low k dielectric material. However Yau et al. teaches forming a pattern of openings (fig. 8D-8F) in said first etch mask layer (514) through said pattern of openings formed in said second layer of low k dielectric material (518); and etching a pattern of openings in said first layer of low k dielectric material (510) through said pattern of openings in said first etch mask layer (514), (col. 12 lines 25-30).

Therefore it would be obvious to one skilled in the at the time of the invention to modify the process of Wang et al. and to pattern openings in said second layer of low k dielectric as taught by Yau et al. because a second dielectric layer is deposited to help pattern openings with the first layer of densified dielectric material.

Claim 11 adds the limitation of the process of claim 10 including forming another etch mask over said second etch mask layer. Wang et al. teaches forming a second dielectric layer over a first etch mask layer. However Wang et al. does not teach forming another etch mask over said second etch mask layer. However Yau et al. teaches forming another etch mask (726) over said second etch mask layer (718), said another mask having openings larger than the openings in said pattern of openings in said second etch mask layer (fig. 10E ref. 24); and etching said larger openings through: said second etch mask layer of densified dielectric material (718); and said second layer of low k dielectric material (722); down to said first etch mask layer of densified dielectric material (714); whereby said structure will have a pattern of smaller openings formed in said first layer (710) of low k dielectric material and a pattern of larger openings formed in said second layer of low k dielectric material and generally in registry with said pattern of smaller openings (fig. 10F, col. 13 lines 11-40). Therefore it would be obvious to one skilled in the art at the time of the invention to modify the process of Wang et al. and to form another etch mask over said second etch mask layer in order to form a dual damascene as taught by Yau et al.

Claim 12 adds the limitation of the process of claim 6 including the further steps of: a) treating the upper surface of said second layer of low k dielectric material to form

a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material; b) patterning said second layer of densified dielectric material to form a second etch mask layer of densified dielectric material over said second layer of low k dielectric material, said second etch mask layer having a pattern of openings therein suitable for use in etching a corresponding pattern of openings in the underlying second layer of low k dielectric material; c) etching a pattern of openings in said second layer of low k dielectric material through said pattern of openings in said second etch mask layer; d) forming a pattern of openings in said first etch mask layer through said pattern of openings formed in said second layer of low k dielectric material; and e) etching a pattern of openings in said first layer of low k dielectric material through said pattern of openings in said first etch mask layer. However, Wang et al. does not teach forming a second layer of densified dielectric material. However Yau et al. teaches treating the upper surface (col. 2 lines 44-50) of said second layer of low k dielectric material (518) to form a second layer of densified dielectric material (522) over the remainder of said second layer of low k dielectric material; patterning said second layer of densified dielectric material to form a second etch mask layer of densified dielectric material (524) over said second layer of low k dielectric material (fig. 8E), said second etch mask layer (524) having a pattern of openings therein suitable for use in etching a corresponding pattern of openings (520) in the underlying second layer of low k dielectric material (518); etching a pattern of openings (520) in said second layer of low k dielectric material (518) through said pattern of openings in said second etch mask layer (fig. 8F); forming a pattern of openings in said first etch mask layer (514) through

said pattern of openings formed in said second layer (518) of low k dielectric material; and etching a pattern of openings (8G) in said first layer of low k dielectric material (510) through said pattern of openings in said first etch mask layer (514). Therefore it would be obvious to one skilled in the art at the time of invention to modify the process of Wang et al. and to form a second layer of densified dielectric material over said second layer of low k dielectric as taught by Yau et al. because the second layer of densified dielectric material has excellent barrier properties and can be used as an etch stop layer.

Claim 13 adds the limitation of the process of claim 12 including the further steps of: a) forming another etch mask over said second etch mask layer, said another etch mask having openings larger than the openings in said pattern of openings in said second etch mask layer. Wang et al. teaches forming an integrated circuit structure (2) having at least one layer of low k material (10) therein and a layer (18), formed from a low k dielectric layer, suitable for use as an etch stop and/or an etch mask. However Wang et al. does not teach forming a second etch mask layer and another etch mask over said second etch mask layer. However, Yau et al. teaches forming another etch mask (726) over said second etch mask layer (716), said another etch mask having openings larger than the openings in said pattern of openings in said second etch mask layer (fig. 10E); and etching said larger openings through: said second etch mask layer; and said second layer of low k dielectric material (718); down to said first etch mask layer (714), using said another etch mask (724); whereby said structure will have a pattern of smaller openings formed in said first layer of low k dielectric material and a

pattern of larger openings formed in said second layer of low k dielectric material and generally in registry with said pattern of smaller openings (fig. 10F, col. 13 lines 40-46). Therefore it would be obvious to one skilled in the art at the time of the invention to modify the process taught by Wang et al. and to form another etch mask over said second etch mask layer in order to form a dual damascene as taught by Yau et al.

Claim 14 adds the limitation of the process of claim 12 wherein said openings formed in said first and second layers of low k dielectric material and said first and second etch mask layers comprise vias and forming a trench mask over said second etch mask layer. Wang et al. teaches forming vias in the first and second layers of low k dielectric and said first etch mask layers. However Wang et al. does not teach a second etch mask. However Yau et al. teaches forming a etch mask (726) over said second etch mask layer (716), said etch mask having openings larger than said vias in said second etch mask layer (fig. 10E); and etching said trenches through: said second etch mask layer; and said second layer of low k dielectric material (718); down to said first etch mask layer (714), whereby said structure will have a pattern of smaller openings formed in said first layer of low k dielectric material and a pattern of trenches formed in said second layer of low k dielectric material, with said trenches in registry with said vias (fig. 10F, col. 13 lines 40-46). Therefore it would be obvious to one skilled in the art at the time of the invention to modify the process of Wang et al. and to form another etch mask over said second etch mask layer in order to form a dual damascene as taught by Yau et al.

Claim 15 adds the limitation to the process of claim 2 including the further steps of: treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material. However Wang et al. does not teach treating the upper surface of said second layer of low k dielectric to form a second layer of densified dielectric material. However Yau et al. teaches forming a second layer of low k dielectric material (518) over said first layer of densified dielectric material (514, col. 12 lines 25-30); treating the upper surface of said second layer of low k dielectric material (518) to form a second layer of densified dielectric material (524), (col. 2 lines 44-50) over the remainder of said second layer of low k dielectric material; and patterning said second layer of densified dielectric material to form a second etch mask layer of densified dielectric material over said second layer of low k dielectric material; said second etch mask layer having a pattern of openings therein comprising openings (520) larger than said openings in said first etch mask layer of densified material (514, fig. 8F), said openings in said second etch mask layer in registry with said openings in said first etch mask layer. Therefore, it would be obvious to one skilled in the art at the time of the invention modify the process of Wang et al. and to deposit a second layer of low k dielectric material over said first layer of densified dielectric material as taught by Yau et al. because a second dielectric layer is deposited to help pattern trenches with the first layer of densified dielectric material. Furthermore, it would be obvious to one skilled in the at the time of the invention to modify the process of Wang et al. and to pattern openings in said second layer of low k dielectric as taught by Yau et al. because a

second dielectric layer is deposited to help pattern openings with the first layer of densified dielectric material.

Claim 16 adds the limitation of the process of claim 2 including the further steps of: forming a second layer of low k dielectric material over said first layer of densified dielectric material; treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material; patterning said second layer of densified dielectric material to form a second etch mask layer of densified dielectric material over said second layer of low k dielectric material, said second etch mask layer having a pattern of openings therein in registry with, but each larger than, said openings formed in said first etch mask layer; etching a pattern of openings in said second layer of low k dielectric material through said pattern of openings in said second etch mask layer, thereby exposing said pattern of openings in said first etch mask layer; and etching a pattern of openings in said first layer of low k dielectric material through said exposed pattern of openings in said first etch mask layer. Wang et al. teaches forming a first and second layer of low k dielectric and treating the upper surface of the first layer of low k to form a first layer of densified dielectric material. However Wang et al. does not teach treating the upper surface of said second layer of low k dielectric to form a second layer of densified dielectric material. However Yau et al. teaches forming a second layer of low k dielectric material (518) over said first layer of densified dielectric material (514); treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material (524) over the remainder of said second

layer of low k dielectric material; patterning said second layer of densified dielectric material to form a second etch mask layer (col. 2 line 50, fig. 8E) of densified dielectric material over said second layer of low k dielectric material, said second etch mask layer having a pattern of openings therein in registry with, but each larger than, said openings formed in said first etch mask layer (fig. 8E); etching a pattern of openings in said second layer of low k dielectric material through said pattern of openings in said second etch mask layer (fig. 8F, ref. 520), thereby exposing said pattern of openings in said first etch mask layer (514); and etching a pattern of openings in said first layer of low k dielectric material through said exposed pattern of openings in said first etch mask layer (fig. 8F, col. 12 lines 32-38). Therefore, it would be obvious to one skilled in the art at the time of the invention to modify the process of Wang et al. and to deposit a second layer of low k dielectric material over said first layer of densified dielectric material as taught by Yau et al. because a second dielectric layer is deposited to help pattern trenches with the first layer of densified dielectric material. Furthermore, it would be obvious to one skilled in the at the time of the invention to modify the process of Wang et al. and to pattern openings in said second layer of low k dielectric as taught by Yau et al. because a second dielectric layer is deposited to help pattern openings with the first layer of densified dielectric material.

Conclusion.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yau et al. (6,245,690) teaches a dual damascene process using low k dielectric etch stop layers.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0957. See MPEP 203.08.

Any inquiry concerning this communication from the examiner should be directed to Lisa Kilday whose telephone number is (703) 306-5728. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry, can be reached on (703) 308-1680. The fax number for the group is (703) 305-3432. MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

Lisa Kilday

LAK

7/26/02

7/29/02

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